


# Voltage-controlled superconducting magnetic memory F

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## ABSTRACT

Over the past few decades, superconducting circuits have been used to realize various novel electronic devices such as quantum bits, SQUIDs, parametric amplifiers, etc. One domain, however, where superconducting circuits fall short is information storage. Superconducting memories are based on the quantization of magnetic flux in superconducting loops. Standard implementations store information as magnetic flux quanta in a superconducting loop interrupted by two Josephson junctions (i.e., a SQUID). However, due to the large inductance required, the size of the SQUID loop cannot be scaled below several micrometers, resulting in low-density memory chips. Here, we propose a scalable memory consisting of a voltage-biased superconducting ring threaded by a half-quantum flux bias. By numerically solving the time-dependent Ginzburg-Landau equations, we show that applying a time-dependent bias voltage in the microwave range constitutes a writing mechanism to change the number of stored flux quanta within the ring. Since the proposed device does not require a large loop inductance, it can be scaled down, enabling a high-density memory technology.

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## I. INTRODUCTION

The quantization of magnetic flux in superconductors lies at the heart of state-of-the-art quantum devices, such as qubits<sup>1</sup> and SQUIDs.<sup>2</sup> When a superconducting loop is placed in an external magnetic field, a persistent supercurrent flows to ensure the total flux enclosed by the loop is an integer multiple of the flux quantum  $\Phi_0 = h/2e$ , where  $h$  is Planck's constant and  $e$  is the electronic charge. As the magnetic field increases, transitions between discrete flux states occur to minimize the free energy of the loop. In general, the quantized flux states of a superconducting loop renders it a suitable candidate for applications in information-storing and processing.

The archetypal superconducting memory stores information as the number of magnetic flux quanta in a SQUID, a superconducting loop interrupted by two Josephson junctions. The size of the SQUID loop, however, cannot be reduced below

several micrometers to allow for a large geometric inductance, resulting in low-density memory chips.<sup>3–5</sup> Because pure superconducting memories proved unscalable, hybrid devices have been investigated by incorporation of nanowires,<sup>6</sup> or semi-conducting<sup>7</sup> and ferromagnetic materials.<sup>8–10</sup> Though promising, these hybrid memories are plagued with various fabrication challenges.<sup>6</sup>

In this paper, we propose a scalable superconducting memory, consisting of three rings. The state of the memory is stored in the vorticity—the winding number of the superconducting order parameter—of an isolated central ring (also referred to as the bit ring). The memory write process occurs via a time-dependent bias voltage that induces transitions between two vorticity states  $N\Phi_0$  and  $(N + 1)\Phi_0$  at a half-integer-flux-quantum bias  $\Phi/\Phi_0 = N + 1/2$ . Using time-dependent Ginzburg-Landau simulations for aluminum nanorings, we demonstrate writing speeds in the order of few picoseconds.

## II. MODEL DESCRIPTION

In this section, we formulate the model for a superconducting magnetic memory. The proposed device is composed of three superconducting rings interconnected via a core with a high magnetic permeability ( $\mu_r \gg 1$ ) in a transformer-like arrangement, as depicted in Fig. 1. The input ring (leftmost in Fig. 1) is used to bias the central/bit ring with a half-flux quantum  $\Phi = \Phi_0/2$ . The number of flux quanta enclosed by the central ring constitutes the memory state, either logic ‘0’ or ‘1’, read by measuring the current circulating in the output/readout ring (rightmost in Fig. 1). The writing process occurs via a pulsed bias voltage applied to the bit ring. Moreover, the device is symmetric; thus, the two side rings can be used interchangeably for bias and readout.

Encoding the memory state, the vorticity of the central/bit ring is given by

$$L \equiv \frac{1}{2\pi} \oint_{\Gamma} \nabla\theta \cdot d\mathbf{l}, \quad (1)$$

where  $\Gamma$  is a circular path inside the ring,  $d\mathbf{l}$  is a differential length element along the azimuthal direction  $\phi$ , and  $\theta$  is the phase of the superconducting order parameter  $\psi = \sqrt{\eta}e^{i\theta}$ . The evolution of the complex order parameter  $\psi$ , in response to a time-varying bias voltage and a constant magnetic flux bias, is obtained using the time-dependent Ginzburg-Landau (GL) equation<sup>11,12</sup>

$$\left(\frac{\partial}{\partial t} + i\kappa V\right)\psi = -\left(\frac{i}{\kappa}\nabla + \mathbf{A}\right)^2\psi + (1 - \eta)\psi, \quad (2)$$

where  $V$  is the electrostatic potential,  $\mathbf{A}$  is the vector potential, and  $\kappa$  is the GL parameter. Equation (2) is written in a dimensionless form where the space coordinate is scaled by the London penetration depth  $\lambda_L$ , and the order parameter by its equilibrium value in the

absence of electromagnetic fields.<sup>13</sup> The time coordinate is scaled by the ratio  $\xi_{GL}^2/\mathcal{D}$  with  $\xi_{GL}$  denoting the GL coherence length and  $\mathcal{D}$  the diffusion coefficient.

Equation (2) is solved self-consistently with the continuity equation  $\nabla \cdot \mathbf{J} = 0$ , which, in the Coulomb gauge, reduces to

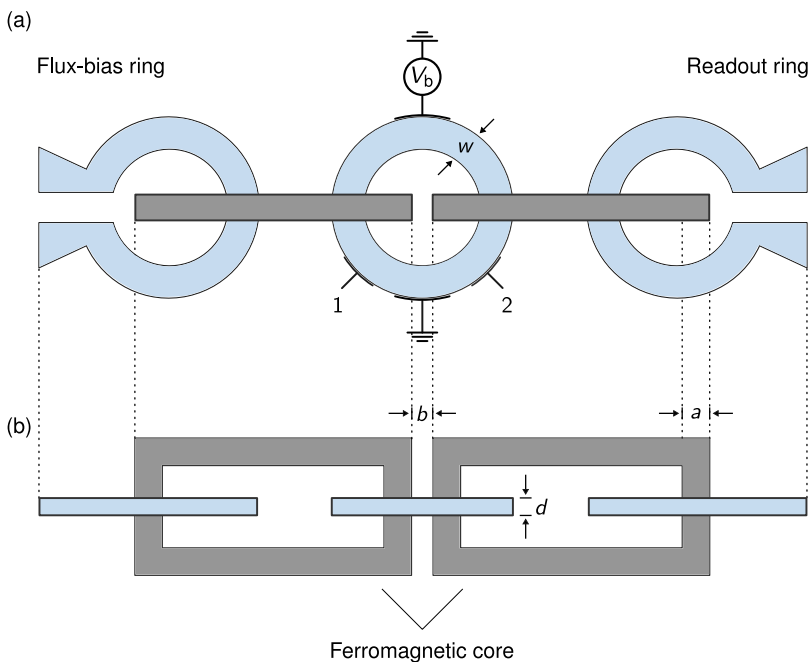
$$\sigma \nabla^2 V = \nabla \cdot \left( \frac{1}{2i\kappa} (\psi^* \nabla \psi - \psi \nabla \psi^*) - \eta \mathbf{A} \right), \quad (3)$$

The dimensionless conductivity  $\sigma$  is given by  $\sigma_n \mathcal{D} \kappa^2 \mu$ , where  $\sigma_n$  is the normal-state conductivity and  $\mu$  is the magnetic permeability.

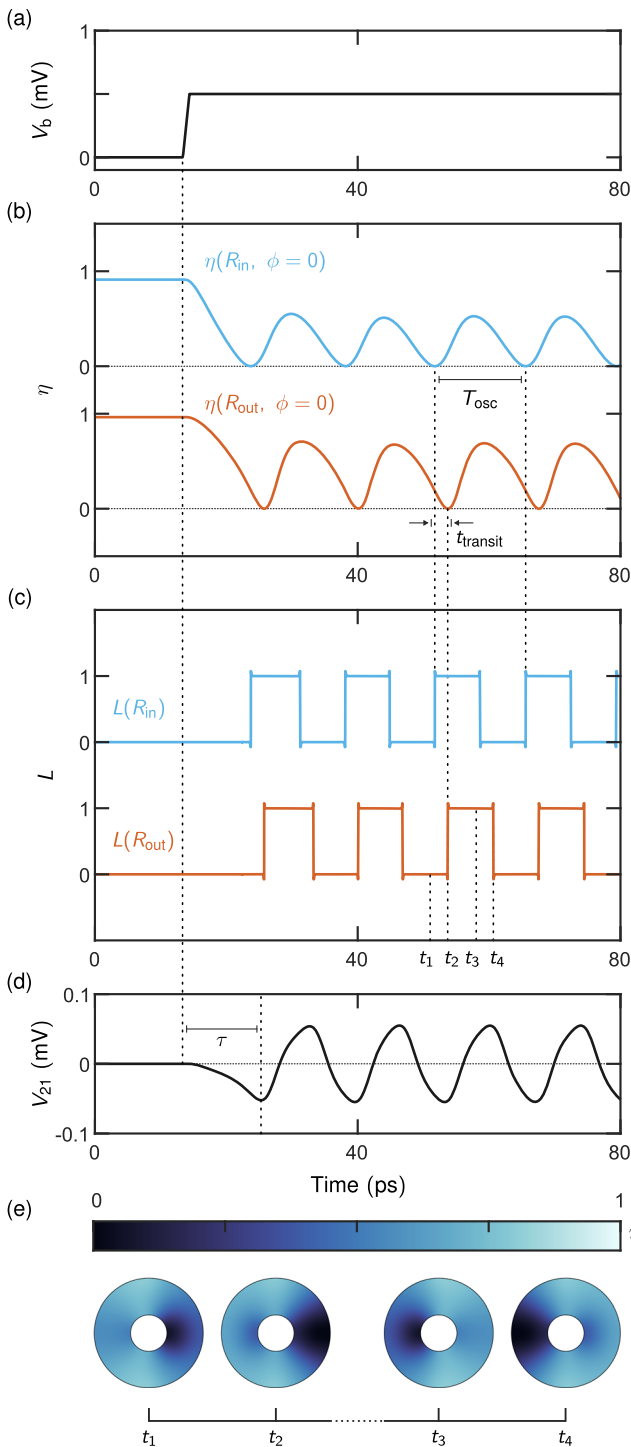
## III. WORKING PRINCIPLE

To demonstrate the working principle of the proposed memory, we consider an aluminum thin-film ring with a resistivity  $\rho_n = 1/\sigma_n = 3.6 \mu\Omega \cdot \text{cm}$ , a mean free path  $\ell = 16 \text{ nm}$  and a critical temperature  $T_c = 1.32 \text{ K}$ .<sup>14</sup> At  $T = 1 \text{ K}$ , the coherence length  $\xi_{GL}(T) = 170 \text{ nm}$ , and the penetration depth  $\lambda_L(T) = 195 \text{ nm}$ . The characteristic time  $\xi_{GL}^2/\mathcal{D}$  is approximately 2.67 ps. The inner radius of the ring  $R_{in}$  equals 195 nm and  $R_{out} = 3R_{in}$ .

The viability of the transformer structure has been experimentally demonstrated in Ref. 15, where the number of flux quanta trapped in the isolated ring is detected by recording the evolution of the critical current of the output ring. One issue, however, that requires further investigation is the scalability of the arrangement. Assuming for simplicity that the cores are of square cross-section with side  $a$  and carry a uniform field, the magnetic induction corresponding to a single-flux quantum is  $B_0 = \Phi_0/a^2$ . The constraint on the side length  $a$  is that both cores should thread the central ring, without touching it nor each other. For the ring under consideration, the inter-core distance  $b$  can be set to 60 nm and the side length  $a$  to



**FIG. 1.** Top (a) and side (b) view of a memory element schematic consisting of three superconducting rings. Two ferromagnetic cores, with a square cross-section of side  $a$ , pierce the central ring, thereby coupling it to two side input/output rings, one is used to bias the bit with a half-integer flux quantum, and the other is used for readout. The inter-core separation distance is denoted by  $b$ . The central ring is of width  $w \equiv R_{out} - R_{in}$ , and is voltage-biased [ $V(R_{out}, 80^\circ \leq \phi \leq 100^\circ) = V_b$ , and  $V(R_{out}, 260^\circ \leq \phi \leq 280^\circ) = 0$ ]. The thickness of the ring  $d$  is much shorter than the GL coherence length  $\xi_{GL}$ ; hence, the model is effectively two-dimensional. Contacts 1 and 2 are used to measure the voltage difference  $V_{12}$  across the ring.



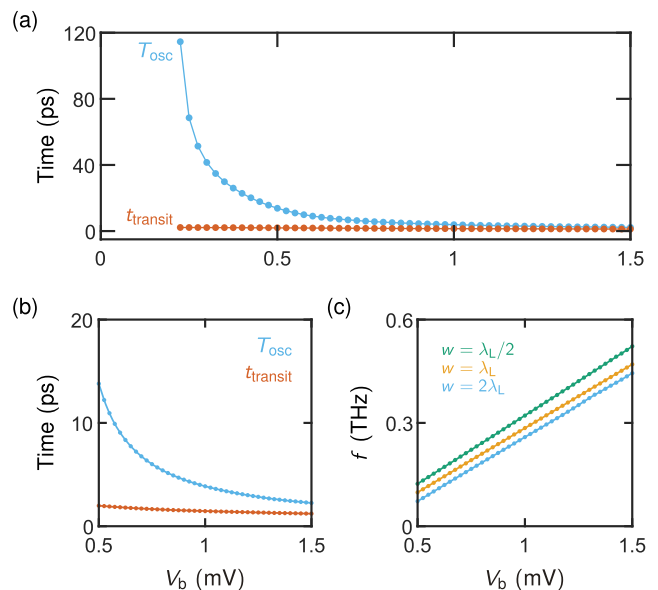
**FIG. 2.** (a) Bias voltage  $V_b$  as a function of time. (b) Normalized Cooper-pair density  $\eta$  at the inner ( $R_{in}$ ) and outer ( $R_{out}$ ) edges of the ring. (c) The vorticity  $L$ , defined in Eq. (1), oscillates as a function of time at a flux bias  $\Phi/\Phi_0 = 1/2$ . (d) Voltage difference between contacts 1 and 2 (Fig. 1) is used to measure the oscillation period  $T_{osc}$ . (e) A transition from  $L = 0$  to  $L = 1$  corresponds to a antivortex departing from the right arm of the ring, whereas the opposite transition corresponds to a vortex departing from the left arm.

145 nm. Accordingly, the magnetic induction  $B_0 \sim 100$  mT, which can be achieved with the ferromagnetic cores.

Importantly, the use of ferromagnetic cores is not the sole possible configuration of the device. For instance, because the flux bias is time-independent, one can place a permanent magnet within the bit ring to generate a half-flux quantum. And the readout process can be realized by use of a SQUID. In the remaining of this paper, the focus is on how the application of a bias-voltage pulse to a superconducting ring, enclosing a concentric half-flux quantum, constitutes a memory write process.

In the absence of bias voltage ( $V_b = 0$ ), the flux quantization, due to the single valuedness of the order parameter, requires that a supercurrent circulate in response to a half-integer magnetic flux bias ( $\Phi = \Phi_0/2$ ). The ground state of the ring then consists of two uncoupled vorticity states, a state  $L = 0$  corresponding to a supercurrent that circulates in a clockwise (cw) direction to oppose the external flux bias, and a state  $L = 1$  corresponding to a counterclockwise (ccw) supercurrent to augment the external flux. Transitions between these two states occur via deterministic phase slips by tuning the free-energy barrier to zero, which requires modulating the magnetic flux bias.

Alternatively, one can control the energy barrier by use of a bias voltage. For the ring depicted in Fig. 1(a), the bias voltage induces two oppositely-circulating currents, a cw current in the right arm and a ccw current in the left arm. Importantly, the current driven by bias voltage interferes with the persistent current due to the half-integer flux bias. For instance, in a state  $L = 0$ , the persistent current circulates in the cw direction, thereby a constructive interference occurs at the right arm of the ring. For a large bias voltage, Cooper pairs are accelerated to their critical superfluid velocity and a phase slip occurs corresponding to a transition from  $L = 0$  to



**FIG. 3.** (a) and (b) Oscillation period  $T_{osc}$  and vortex transit time  $t_{transit}$  as a function of bias voltage  $V_b$  for a ring of width  $w = 2\lambda_L$ . (c) Frequency  $f$  in terahertz as a function of bias voltage for  $w = 0.5, 1$ , and  $2\lambda_L$ . For a given bias voltage, the frequency is higher for a ring of a smaller width.

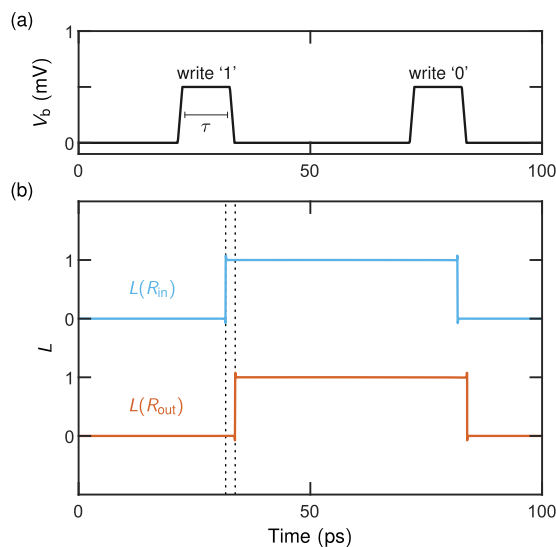
$L = 1$  [Fig. 2(c)]. In contrast, in the flux state  $L = 1$ , the phase slip occurs in the left arm corresponding to a transition from  $L = 1$  to  $L = 0$ . Accordingly, the vorticity of the ring oscillates between  $L = 0$  and  $L = 1$ , implying a zero free-energy barrier between the two vortex states in the presence of bias voltage.

Importantly, one can harness the magnetic bistability of the central ring to realize a memory bit. Instead of a constant bias, a time-dependent voltage is used to temporarily lower the free-energy barrier to allow for a single transition, constituting a memory write process. In the next section, we investigate the required pulse width and height, along with the resulting writing speed as a function of the bias voltage and ring dimensions.

#### IV. CHARACTERIZATION

Before addressing the memory write, it is insightful to analyze the oscillation frequency as a function of the bias voltage. As shown in Fig. 2, the oscillation period  $T_{\text{osc}}$ , defined as the time difference between two consecutive minima of the Cooper-pair density at the same point in the ring, can be extracted experimentally by measuring the voltage difference  $V_{12}$  (Fig. 1). For a small bias voltage, the velocity of Cooper pairs is less than the critical superfluid velocity, and no oscillations occur (Fig. 3). As the bias voltage increases, Cooper pairs are accelerated to the critical velocity in a shorter time; hence, the frequency increases linearly, and, for the ring under consideration, it is in the order of a terahertz [Fig. 3(c)]. Moreover, at a given bias voltage, the oscillation frequency is higher for a smaller width of the ring.

Importantly, the oscillation period decreases asymptotically towards the vortex transit time  $t_{\text{transit}}$ —the time it takes a vortex to cross the superconducting ring (see Fig. 2). In the limit  $T_{\text{osc}} \sim t_{\text{transit}}$ ,



**FIG. 4.** (a) Bias voltage  $V_b$  in mV as a function of time in picoseconds. The pulse width  $\tau$  is chosen based on Fig. 2(d). (b) Memory state, i.e., the vorticity  $L$ , as a function of time.

a vortex is formed at the inner rim of the ring before the previous one completely leaves. Therefore, it is impractical to use a time-dependent bias voltage to allow for only a single transition between the two vortex states.

Having determined the desired operational bias voltage, i.e., the pulse height, we obtain the recipe for the pulse width from Fig. 2(d). In particular, the bias voltage is ramped to its steady-state value, while measuring the voltage difference  $V_{12}$ . The pulse duration  $\tau$  is chosen as the difference between the instant the bias voltage is switched on and the first peak in  $V_{12}$ .

Using the determined pulse width and height, the same bias voltage can be used to write logic '0' and '1', as shown in Fig. 4. In particular, in the presence of a half-integer flux bias  $\Phi/\Phi_0 = N + 1/2$ , the bias-voltage pulse induces a transition from an initial state  $L = N$  to  $L = N + 1$ , corresponding to writing logic '1'. Reapplying the same pulse results in a phase slip in the other arm of the ring, corresponding to writing logic '0'. The memory state is maintained as long as the ring is in the superconducting state because the circulating supercurrent persists for years, as shown in various experiments.<sup>13</sup>

#### V. CONCLUSIONS

In this paper, we have proposed a memory element consisting of three superconducting rings interconnected via a two ferromagnetic cores. Using time-dependent GL simulations, we have demonstrated the use of bias voltage as a writing mechanism. For aluminum nanorings, the writing speed is in the order of few picoseconds.

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